IN THE CLAIMS

1. (Currently Amended) A double-edge-trigger-flip-flop comprising:

a first pass gate controlled by a clock signal and an inverted signal of the clock signal for passing an input;

a second pass gate controlled by the clock signal and the inverted signal of the clock signal for passing the input in a complementary manner with regard to the first pass gate;

a first signal passing module for further passing the input passed by the first pass gate into a third pass gate controlled by the clock signal for and the inverted signal of the clock signal for generating a first part of an output of the flip-flop, wherein the third pass gate passes ~~the input~~ an output of the first signal passing module in a complementary manner with regard to the first pass gate; and

a second signal passing module for further passing the input passed by the second pass gate into a fourth pass gate controlled by the clock signal and the inverted signal of the clock signal for generating a second part of the output, wherein the fourth pass gate passes ~~the input~~ an output of the second signal passing module in a complementary manner with regard to the second pass gate

wherein at least one of the first or the second signal passing module is a NAND gate.

2. (Currently Amended) The flip-flop of claim 1 further comprising a driver module ~~passing~~ for providing the first part of the output on a first edge of the clock input and ~~passing~~ for providing the second part of the output on a second edge of the clock input.

3. (Original) The flip-flop of claim 1 wherein the first signal passing module and the second signal passing module are inverters.

4. (Currently Amended) The flip-flop of claim 1 wherein each of the first signal passing module and the second signal ~~are NAND gates~~ is a NAND gate for receiving a flag signal together with the passed input wherein the flag signal ~~disenables~~ disables the flip-flop when ~~it~~ the flag signal is asserted.

5. (Currently Amended) The flip-flop of claim 1 wherein each of the first and fourth pass gates ~~have~~ further comprise a PMOS transistor and an NMOS transistor connected in parallel ~~for passing the input with~~ and wherein the PMOS ~~transistors thereof~~ transistor is controlled by the clock signal ~~input~~ and the NMOS ~~transistors thereof~~ transistor is controlled by the inverted signal of the clock signal ~~input~~.

6. (Currently Amended) The flip-flop of claim 1 wherein each of the second and third pass gates ~~have~~ further comprise a PMOS transistor and an NMOS ~~transistors~~ transistor connected in parallel ~~for passing the input with~~ and wherein the NMOS

transistors ~~thereof~~ is controlled by the clock input and the PMOS ~~transistors~~ transistor ~~thereof~~ is controlled by the inverted signal of the clock signal ~~input~~.

7. (Currently Amended) A double-edge-trigger flip-flop comprising:

a first pass gate passing an input when a clock input having a low value;

a second pass gate passing the input when the clock input having a high value;

a first signal passing module for further passing the input passed by the first pass gate into a third pass gate which passes ~~the input~~ an output of the first signal passing module when the clock input has ~~a~~ the high value to generate a first output;

a second signal passing module for further passing the input passed by the second gate into a fourth pass gate which passes ~~the input~~ an output of the second signal passing module when the clock has a low value to generate a second output; and

a driver module ~~passing~~ for providing the first output as an output of the flip-flop on the rising edge of the clock input and ~~passing~~ for providing the second output as the output of the of the flip-flop on the falling edge of the clock input

wherein at least one of the first or the second signal passing module is a NAND gate.

8. (Original) The flip-flop of claim 7 wherein the first signal passing module an the second signal passing module are inverters.

9. (Currently Amended) The flip-flop of claim 7 wherein each of the first signal passing module and the second signal ~~are NAND gates~~ is a NAND gate for receiving a flag signal together with the respective passed input wherein the flag signal ~~disenables~~ disables the flip-flop when ~~it~~ the flag signal is asserted.

10. (Currently Amended) The flip-flop of claim 7 wherein each of the first and fourth pass gates ~~have~~ further comprise a PMOS transistor and an NMOS transistor connected in parallel ~~for passing the input with~~ and wherein the PMOS ~~transistors thereof~~ transistor is controlled by the clock input and the NMOS ~~transistors thereof~~ transistor is controlled by an inverted signal of the clock signal ~~input~~.

11. (Currently Amended) The flip-flop of claim 7 wherein each of the second and third pass gates ~~have~~ further comprise a PMOS transistor and an NMOS transistor ~~transistors~~ connected in parallel ~~for passing the input with~~ and wherein the NMOS ~~transistors~~ transistor ~~thereof controlled~~ is by the clock signal ~~input~~ and the PMOS ~~transistors thereof controlled~~ transistor is controlled by an inverted signal of the clock signal ~~input~~.

12. (Currently Amended) A double-edge-trigger flip-flop comprising:

a first pass gate controlled by a clock signal and an inverted signal of the clock signal for passing an input;

a second pass gate controlled by the clock signal and the inverted signal of the clock signal for passing the input in a complementary manner with regard to the first pass gate;

a first signal passing module for further passing the input passed by the first pass gate into a third pass gate controlled by the clock signal and the inverted signal of the clock signal for generating a first part of an output of the flip-flop, wherein the third pass gate passes ~~the input~~ an output of the first passing module in a complementary manner with regard to the first pass gate;

a second signal passing module for further passing the input passed by the second pass gate into a fourth pass gate controlled by the clock signal and the inverted signal of the clock signal for generating a second part of the output, wherein the fourth pass gate passes ~~the input~~ an output of the second signal passing module in a complementary manner with regard to the second pass gate; and

a driver module ~~passing~~ for processing the first part of the output on a first edge of the clock signal ~~input~~ and ~~passing~~ further processing the second part of the output on a second edge of the clock signal ~~input~~,

wherein each of the first and fourth pass gates ~~have~~ further comprise a PMOS transistor and an NMOS transistor connected in parallel ~~for passing the input with~~ and wherein the PMOS ~~transistors thereof~~ transistor is controlled by the clock ~~input~~ signal and the NMOS ~~transistors thereof~~ transistor is controlled by the inverted signal of the clock signal ~~input~~, and

wherein each of the second and third pass gates further comprise ~~have~~ a PMOS transistor and an NMOS ~~transistors~~ transistor connected in parallel ~~for passing the input with~~ and wherein the NMOS ~~transistors thereof controlled~~ transistor is controlled by the clock ~~input~~ signal and the PMOS ~~transistors thereof~~ transistor is controlled by the inverted signal of the clock signal ~~input~~

wherein at least one of the first or the second signal passing module is a NAND gate.

13. (Original) The flip-flop of claim 12 wherein the first signal passing module and the second signal passing module are inverters.

14. (Currently Amended) The flip-flop of claim 12 wherein each of the first signal passing module and the second signal ~~are NAND gates~~ is a NAND gate for receiving a flag signal together with the respective passed input.

15. (Currently Amended) A method for passing an input signal through a double-edge-trigger flip-flop, the method comprising:

passing ~~an~~ the input signal through a first pass gate controlled by a clock signal and an inverted signal of the clock signal;

passing the input through a second pass gate controlled by the clock signal and the inverted signal of the clock signal in a complementary manner with regard to the first pass gate;

~~passing~~ processing the input passed by the first pass gate ~~through~~ by using a first signal passing module;

passing ~~the input passed by~~ an output of the first signal passing module ~~to~~ through a third pass gate controlled by the clock signal and the inverted signal of the clock signal for generating a first part of an output of the flip-flop, wherein the third pass gate passes ~~the input~~ an output of the first signal passing module in a complementary manner with regard to the first pass gate;

~~passing~~ processing the input passed by the second pass gate ~~through~~ by using a second signal passing module;

passing ~~the input passed by~~ an output of the second signal passing module ~~to~~ through a fourth pass gate controlled by the clock signal and the inverted signal of the clock signal for generating a second part of the output, wherein the fourth pass gate passes ~~the input~~ the output of the second passing module in a complementary manner with regard to the second pass gate,

wherein the first and second parts of the output are produced upon two edges of the clock signal sequentially

wherein at least one of the first or the second signal passing module is a NAND gate.

16. (Currently Amended) The method claim 15 further comprising ~~passing~~ processing the first and second parts of the output through a driver module.

17. (Original) The method claim 16 wherein the driver module is an inverter.

18. (Original) The method claim 15 wherein the first signal passing module and the second signal passing module are inverters.

19. (Currently Amended) The method claim 15 wherein each of the first signal passing module and the second signal ~~are NAND gates~~ is a NAND gate for receiving a flag signal together with the respective passed input wherein when the flag signal ~~disenables~~ disables the flip-flop when ~~it~~ the flag signal is asserted.

20. (Currently Amended) The method claim 15 wherein each of the first and fourth pass gates ~~have~~ further comprise a PMOS transistor and an NMOS transistor connected in parallel ~~for passing the input with~~ and wherein the PMOS ~~transistors thereof~~ transistor is controlled by the clock signal ~~input~~ and the NMOS ~~transistors thereof~~ transistor is controlled by the inverted signal of the clock signal ~~input~~, and wherein each of the second and third pass gates have a PMOS transistor and an NMOS transistor ~~transistors~~ connected in parallel ~~for passing the input with~~ and wherein the NMOS ~~transistors~~

~~thereof~~ transistor is controlled by the clock ~~input~~ signal and the PMOS ~~transistors thereof~~ transistor is controlled by the inverted signal of the clock signal ~~input~~.

21. (New) A double-edge-trigger-flip-flop comprising:

a first pass gate controlled by a clock signal and an inverted signal of the clock signal for passing an input;

a second pass gate controlled by the clock signal and the inverted signal of the clock signal for passing the input in a complementary manner with regard to the first pass gate;

a first signal passing module for further passing the input passed by the first pass gate into a third pass gate controlled by the clock signal for and the inverted signal of the clock signal for generating a first part of an output of the flip-flop, the third pass gate passes an output of the first signal passing module in a complementary manner with regard to the first pass gate;

a second signal passing module for further passing the input passed by the second pass gate into a fourth pass gate controlled by the clock signal and the inverted signal of the clock signal for generating a second part of the output, wherein the fourth pass gate passes an output of the second signal passing module in a complementary manner with regard to the second pass gate; and

wherein each of the first signal passing module and the second signal is a NAND gate for receiving a flag signal together with the passed input wherein the flag signal disables the flip-flop when the flag signal is asserted.

22. (New) A double-edge-trigger flip-flop comprising:

a first pass gate passing an input when a clock input having a low value;

a second pass gate passing the input when the clock input having a high value;

a first signal passing module for further passing the input passed by the first pass gate into a third pass gate which passes an output of the first signal passing module when the clock input has the high value to generate a first output;

a second signal passing module for further passing the input passed by the second gate into a fourth pass gate which passes an output of the second signal passing module when the clock has a low value to generate a second output;

a driver module for providing the first output as an output of the flip-flop on the rising edge of the clock input and for providing the second output as the output of the of the flip-flop on the falling edge of the clock input; and

wherein each of the first signal passing module and the second signal is a NAND gate for receiving a flag signal together with the respective passed input wherein the flag signal disables the flip-flop when the flag signal is asserted.

23. (New) A double-edge-trigger flip-flop comprising:

a first pass gate controlled by a clock signal and an inverted signal of the clock signal for passing an input;

a second pass gate controlled by the clock signal and the inverted signal of the clock signal for passing the input in a complementary manner with regard to the first pass gate;

a first signal passing module for further passing the input passed by the first pass gate into a third pass gate controlled by the clock signal and the inverted signal of the clock signal for generating a first part of an output of the flip-flop, wherein the third pass gate passes an output of the first passing module in a complementary manner with regard to the first pass gate;

a second signal passing module for further passing the input passed by the second pass gate into a fourth pass gate controlled by the clock signal and the inverted signal of the clock signal for generating a second part of the output, wherein the fourth pass gate passes an output of the second signal passing module in a complementary manner with regard to the second pass gate;

a driver module for processing the first part of the output on a first edge of the clock signal and further processing the second part of the output on a second edge of the clock signal,

wherein each of the first and fourth pass gates further comprise a PMOS transistor and an NMOS transistor connected in parallel and wherein the PMOS transistor is

controlled by the clock signal and the NMOS transistor is controlled by the inverted signal of the clock signal,

wherein each of the second and third pass gates further comprise a PMOS transistor and an NMOS transistor connected in parallel and wherein the NMOS transistor is controlled by the clock signal and the PMOS transistor is controlled by the inverted signal of the clock signal; and

wherein each of the first signal passing module and the second signal is a NAND gate for receiving a flag signal together with the respective passed input.

24. (New) A method for passing an input signal through a double-edge-trigger flip-flop, the method comprising:

passing the input signal through a first pass gate controlled by a clock signal and an inverted signal of the clock signal;

passing the input through a second pass gate controlled by the clock signal and the inverted signal of the clock signal in a complementary manner with regard to the first pass gate;

processing the input passed by the first pass gate by using a first signal passing module;

passing an output of the first signal passing module through a third pass gate controlled by the clock signal and the inverted signal of the clock signal for generating a

first part of an output of the flip-flop, wherein the third pass gate passes an output of the first signal passing module in a complementary manner with regard to the first pass gate;

processing the input passed by the second pass gate by using a second signal passing module;

passing an output of the second signal passing module through a fourth pass gate controlled by the clock signal and the inverted signal of the clock signal for generating a second part of the output, wherein the fourth pass gate passes the output of the second passing module in a complementary manner with regard to the second pass gate,

wherein the first and second parts of the output are produced upon two edges of the clock signal sequentially; and

herein each of the first signal passing module and the second signal is a NAND gate for receiving a flag signal together with the respective passed input wherein when the flag signal disables the flip-flop when the flag signal is asserted.